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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,928	03/31/2001	John T. Orchard	15685P096	7550

8791 7590 02/27/2004

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EXAMINER

NGO, CHUONG D

ART UNIT	PAPER NUMBER
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2124

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/823,928

Applicant(s)

ORCHARD, JOHN T.

Examiner

Chuong D Ngo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 13 January 2002.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 2-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grisamore (6,535,901).

As per claims 2,3,11,12,14-18,26,27 and 29-31, Grisamore discloses in figures 5 and 9 a method for implementing a Wallace-architecture in which full-adders (3-dot circle) and half adders (2-dot circle) are selected and their numbers are clearly depend on a bit-wise analysis of the input terms within each level of bit-significance. It is noted that Grisamore does not teach registers in figures 5 and 9. However, Grisamore discloses that it is known in the art to use registers at optimal points in a multiplier to enable pipelined processing which provides a high through put multiply accumulate circuit. Thus it would have been obvious to a person of ordinary skill in the art to provides the Wallace-architecture of Grisamore with registers at optimal points in the architecture to enable pipelined processing in order increase the through put of circuit.

As per claims 4,13,19-25 and 28, since it is well know in the art to implement a multiplier by a FPGA (see the cited references), It would have been obvious to a person of

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ordinary skill in the art, as a matter of design choice, to implement the multiplier by a FPGA as claimed.

3. Claims 2-31 rejected under 35 U.S.C. 103(a) as being unpatentable over Costa et al. (5,935,201).

As per claims 2,3,11,12,14-18,26,27 and 29-31, Costa et al. discloses in figures 7-9 a Wallace-architecture in which full-adders (3-input block) and half adders (2-input block) are selected and their numbers are clearly depend on a bit-wise analysis of the input terms within each level of bit-significance. It is noted that Costa et al does not teach registers in the Wallace-architecture. However, since it is known in the art to use registers at optimal points in a multiplier to enable pipelined processing which provides a high through put multiply circuit. Thus, it would have been obvious to a person of ordinary skill in the art to provides the Wallace-architecture of Costa et al. with registers at optimal points in the architecture to enable pipelined processing in order increase the through put of circuit.

As per claims 4,13,19-25 and 28, since it is well know in the art to implement a multiplier by a FPGA (see the cited references), It would have been obvious to a person of ordinary skill in the art, as a matter of design choice, to implement the multiplier by a FPGA as claimed.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong D Ngo whose telephone number is (703) 305-9764. The examiner can normally be reached on Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 309-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Chuong D Ngo  
Primary Examiner  
Art Unit 2124

02/20/2004